## REMARKS

Claims 1-21 are pending. Claims 1, 7, 11, 13, 15, and 17-19 have been amended. Claim 16 has been canceled.

**Interview Summary**

The undersigned wishes to thank Examiner Thomas and Supervisory Examiner Werner for taking the time to conduct a telephonic interview on August 8, 2007. During the interview, the undersigned presented the arguments set forth below concerning the Section 102(b) rejection. The meaning of the term "GPU" was discussed as opposed to a video codec type processing component. The Applicants have provided further definition of how the processing in the instant invention is distinctive over video codec type processing in this response. No agreement was reached, although the Examiner indicated that she would further consider this written response.

**Regarding the Claim Objections under 37 CFR 1.75(a)**

Claims 2 and 14 have been amended as suggested by the Examiner to overcome the rejection under 37 CFR 1.75(a). Reconsideration is therefore respectfully requested.

**Regarding the Rejections under 35 U.S.C. §112**

Claim 15 has been amended to more particularly point out and distinctly claim the subject matter of the invention. The applicants submit that, as amended, the claim satisfies the requirements of 35 U.S.C. §112. Reconsideration of the Section 112 rejection of the claim is respectfully requested.

**Regarding the Rejections under 35 U.S.C. §102**

Claims 1-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Chow et al (US 6,292,589). These rejections are respectfully traversed.

Regarding claims 1, 7, 11, 13 and 15, the claims now each recite that the relevant processing is performed by a "shader module." For example, claim 1 recites that "wherein said multiplying … , determining, and sampling the pixels are performed by a shader

module," claim 7 recites that "said creating a polyline and creating a line are performed by a shader module," and claim 11, 13 and 15 recite that "said multiplying ... and adding are performed by a shader module." In order to anticipate a claim, the reference must teach every element of the claim. The Office Action appears to assert that the Chow et al reference teaches these features in column 45, line 41 and Figures 2, 28 and/or 31A of the reference, however, it does not.

At column 45, line 41 and Figure 31A, the Chow et al reference teaches the manipulation of pixel data within a processor. This process is a straightforward compression/decompression process using a video codec type processor. However, the Chow et al reference does not teach or imply that pixel operations other than basic high-speed I/O operations are performed outside of the central processing unit CPU, as is recited in claims 1, 7, 11, 13, and 15. In fact, the Chow et al reference discloses, in column 8, lines 6-51, that the processor within the system may actually drop incoming frames of pixels when they are received too quickly for the video codec to process rather than distributing the incoming frames to additional processor resources separate from the CPU. The Chow et al reference recites the very condition that the instant claims resolve.

The instant invention recites a shader module used in association with a discrete cosine transformation (DCT) algorithm to process incoming 8x8 blocks of pixels by forming a cross product with an orthogonal matrix to preserve the values of the incoming pixels quickly in block and matrix dot product sets. These sets are preserved as textured lines and scanlines and stored into memory quickly, thus eliminating pixel loss. The input video data capture process is therefore greatly enhanced. To process this incoming data prior to delivery to a CPU or an output process, a shader module is employed using the correct matrix values and array offsets to allow DCT processing of each group of textured lines and scanlines as parallel processes. This process improves not only data capture but also improves processing speed for all pixels within the captured video data.

The Chow et al reference makes no provision for distributing portions of the pixel processing activity, other than straightforward compression/decompression actions, outside of the CPU. Providing this processing functionality as a shader process within a processing unit of any type, as is recited in claims 1, 7, 11, 13 and 15, allows for processing of incoming

pixel data in the GPU to offload the CPU and avoid the loss of data that is represented by the dropped frames referenced in column 8 of the Chow et al reference.

In addition, the apportionment of shader processing activities requires coordination between the CPU and GPU in order to synchronize operations such that the two processing entities work together to complete all processing activities in parallel without loss of data. The reference is silent as to any such coordination or apportionment of activities between the CPU and GPU, and Figure 28 does not remedy this silence. Therefore, the Chow et al reference does not anticipate claims 1, 7, 11, 13, and 15 as recited. Accordingly, reconsideration and allowance are respectfully requested.

Regarding claims 3-6, 8-9, 12, 15, and 17-21, these claims each depend from one of independent claims 1, 7, 11, 13 or 15. In view of the above, it is clear that Chow et al fails to establish anticipation of these claims. The dependant claims are, therefore, allowable for at least the reasons shown for claims 1, 7, 11, 13 and 15. Accordingly, reconsideration and allowance are respectfully requested.

## CONCLUSION

For the foregoing reasons, Applicants respectfully submit that the instant application is in condition for allowance.

Respectfully submitted,

Date: August 9, 2007

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